https://chipaitech.com/careers/dft-engineer-senior-lead/

DFT Engineer / Senior / Lead

Hiring organization
chipai tech

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Description

About ChipAI

ChipAI is a semiconductor engineering services company delivering design, verification, physical design, DFT, foundation IP, post-silicon, embedded and software solutions for global technology companies. Our DFT team works on complex SoCs and IPs at advanced process nodes, from architecture through silicon bring-up.

Role overview

We are looking for DFT engineers at all levels to define, implement and validate test architectures for complex SoC and IP designs. Depending on experience, you will own blocks, lead subsystems, or define chip-level DFT strategy and lead teams.

Responsibilities

- Define and implement DFT architecture for SoC and IP designs, including scan, compression, MBIST, JTAG/boundary scan and IJTAG.
- Perform scan insertion and compression (EDT/SSN) and integrate DFT logic at RTL and gate level.
- Run DFT design rule checks (Spyglass DFT or equivalent) and resolve testability issues early in the flow.
- Generate and optimize ATPG patterns for stuck-at, transition, path-delay and bridging faults, meeting coverage and test-time targets.
- Implement and verify MBIST with and without repair, including BIRA/BISR.
- Develop DFT timing constraints for scan shift and capture modes, and support STA and timing closure.
- Perform gate-level simulation (with and without timing) and debug pattern failures.
- Run logic equivalence checks (LEC) on DFT-inserted netlists.
- Support silicon bring-up, ATE pattern debug, fail-log diagnosis and yield analysis.
- Automate DFT flows using Tcl, Perl or Python.
- Collaborate with RTL, physical design, STA and test engineering teams, and with customers.

Additional expectations by level

Level
Experience
Focus

DFT Engineer
2–5 years
Block-level scan insertion, ATPG, simulations and DRC fixes under guidance

Senior DFT Engineer
5–10 years

Full ownership of block or subsystem DFT, coverage and test-time goals, mentoring juniors

Lead DFT Engineer
10–15 years
SoC-level DFT architecture, test planning, leading teams of 5–15 engineers, customer interface

Required skills

- Strong fundamentals in DFT concepts: scan, compression, ATPG fault models, MBIST and boundary scan.
- Hands-on experience with industry-standard DFT tools (Siemens Tessent, Synopsys TestMAX/DFTMAX, Cadence Modus, or equivalent).
- Experience with ATPG coverage analysis and pattern debug.
- Working knowledge of Verilog/SystemVerilog, synthesis, STA and LEC.
- Scripting in Tcl, Perl or Python.
- Good debugging, communication and teamwork skills.

Good to have

- Experience at advanced nodes (7 nm and below).
- SSN, IJTAG (IEEE 1687), LBIST or in-system test experience.
- Silicon bring-up, ATE and yield-analysis exposure.
- Experience with hierarchical DFT on large SoCs.
- Exposure to AI-assisted or automated DFT flows.

Qualifications

B.E./B.Tech or M.E./M.Tech in Electronics, Electrical, VLSI or a related field.

Job Benefits

- Work on complex, next-generation semiconductor programs for global customers.
- Clear growth paths from engineer to technical or people leadership.
- Mentoring from experienced DFT leaders and a strong learning culture.
- A collaborative, engineering-first environment.

Contacts

Send your resume to hr@chipaitech.com or sudarshan.ganji@chipaitech.com with the subject line “DFT Engineer – [Years of experience]”.