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RTL-ASIC Engineer

Hiring organization
chipai tech

Job Location
Bangalore

Date posted
November 16, 2026

Experience
3+ Years

Responsibilities

- Strong experience in RTL design using Verilog and SystemVerilog.
- Hands-on expertise across the complete ASIC RTL design flow, from specification and microarchitecture definition to RTL development, verification, timing analysis, DFT, and implementation.
- Experience with RTL integration, sign-off tools, UPF/low-power verification, CDC/RDC analysis, and lint checks.
- Strong understanding of clocking architectures, system modes, power management, debugging, interconnects, safety, security, and related SoC architectures.

Contacts
Interested candidates can share their updated resumes at **hr@chipaitech.com**